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DESIGN AND IMPLEMENTATION OF SYNTHESIZABLE SPACEWIRE CORES

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Presentation goals

- Introduce Space Research Group (SRG)
- Design and implementation of synthesizable spacewire cores

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Space Research Group

- University of Alcalá http://www.srg.uah.es
- Two divisions:
  - Scientific, Department of Physics
  - Technical, Department of Computer Engineering
- Capabilities:
  - Solar physics research
  - Mission planning and ground systems
  - Test development tools
  - ***On board software development***
  - ***On board electronics development***

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Space Research Group Activities

On board satellite instrumentation (Electronics and SW)

- Hardware: processors, FPGAs, buses, etc.
- Hardware/Software Codesign
- Embedded systems
- Real time operating systems
- High reliability software development (Ada, C/C++, Java)
  - ESA standard PSS05
  - IEEE standards
- Object Oriented SW development tools (EDROOM, HRTHOOD)
- Planning & Scheduling

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Space Research Group Projects

Finished:

- SOHO: CDPU CEPAC consortium
- PHOTON: PESCA instrument
- FUEGO 2: OBDH and fligth software
- NanoSat 01: fligth software and maintenance

In progress:

- NanoSat 1b: fligth software
- Microsat: OBDH, RTUs, EGSE and fligth SW
- Solar Orbiter: LVPS and CDPU for EPD experiment
- ExoMars: Autonomous Navigation Software Porting to RTEMS Leon 2 Platform

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IP Library Development

- Synthesizable IP cores
  - RTU
  - CAN bus
  - TTC.B.01
  - MIL STD 1553
  - SpaceWire, ….

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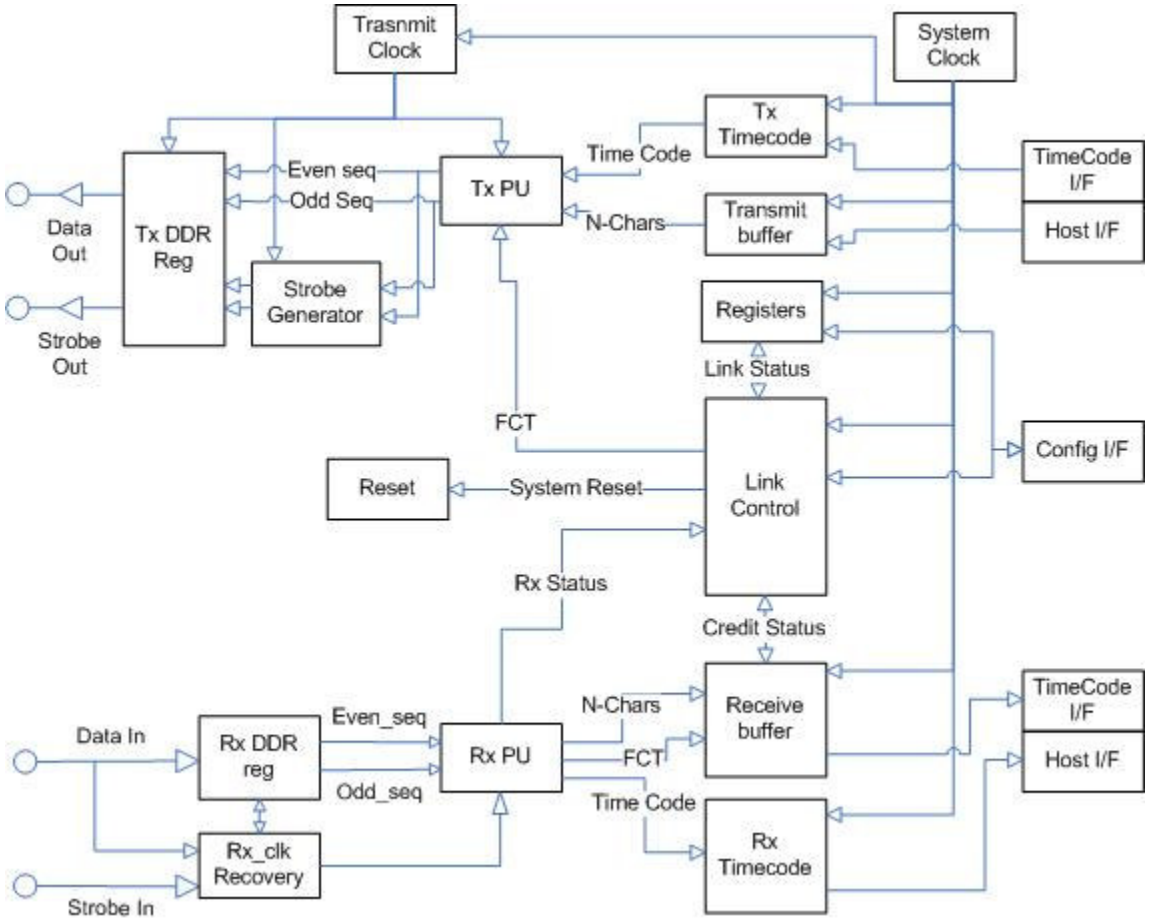
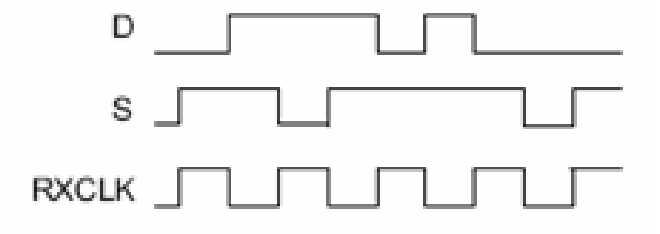
Spacewire IP Core

- Based in ECSS-E50-12A ESA Standard (from scratch)
- Synthesizable SpaceWire CODEC and router.
- Implemented on Xilinx and Actel devices
- Tested with StarDundee Ltd. commercial equipment (PCI2 board and USBbrick)

SpaceWire CODEC (I)

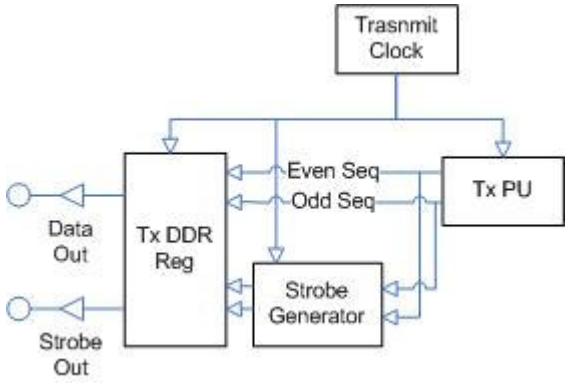


SpaceWire CODEC (II)



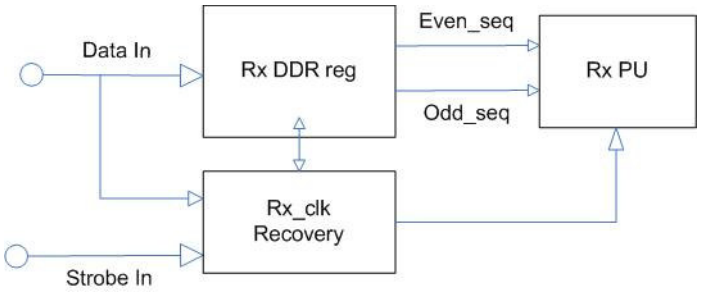
$$S_{even} = D_{even} \oplus 1 = \overline{D_{even}}$$

$$S_{odd} = D_{odd} \oplus 0 = D_{odd}$$



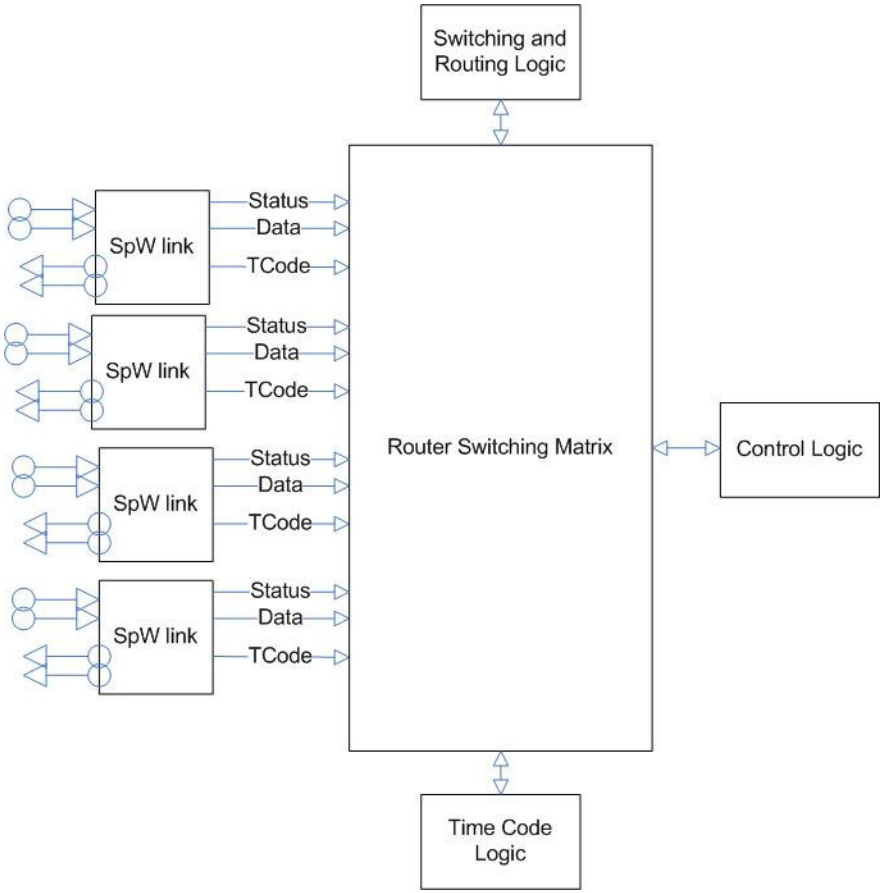
- Tx Strobe Signal Generation:
  - Based in Rx_clock Xoring properties .
  - From even and odd data sequencies.
  - Both sequencies are DDR combined to obtain Strobe output signal.
  - Path delay equalization using flip flops

SpaceWire CODEC (III)



- Rx even and odd sequencies processing:
  - Even seq. rising edge synchronised.
  - Odd seq. falling edge synchronised.
  - Procesed separated, results are merged.
  - Taking advantage of half cycle lag at even seq.
  - Result: serial to paralel conversion

SpaceWire Router (II)



- Independent entity (structural approach).
- Basic approach: 4 nodes, WH routing, fixed LA.
- Up to 8 links (limit: FPGA resources)
- Generics based configuration (at synthesis)

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Development and Testing

- Vital models from Actel and Xilinx. (postlayout testing)
- STAR-Dundee Ltd SpW PCI2 (Codec Prototype)
- STAR-Dundee Ltd SpW USB Brick (Network test)

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Future Works

- Advanced codec host I/F: RMAP, DMA transfers …
- Improve router design: GAR, RMAP, addressing schemes, …
- PCB board design.

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Acknowlegments

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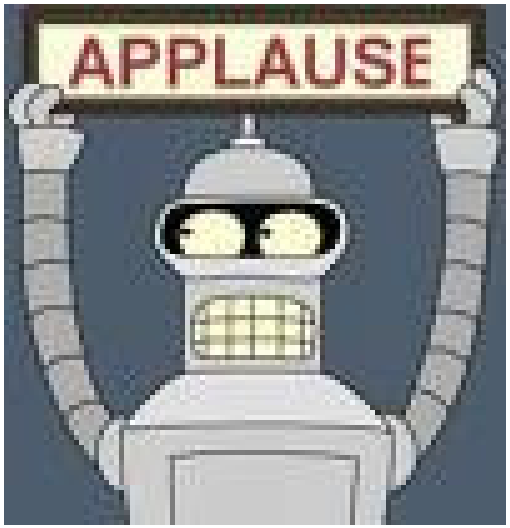
Thanks For Your Attention !



Any Question?